ELECTRONIC INFORMATION DISCLOSURE STATEMENT

Electronic Version v18

Stylesheet Version v18.0

Title of Invention	Integrated Circuit Chip Having A Ringed Wiring Layer Interposed Between A Contact Layer And A Wiring Grid

Application Number :

Confirmation Number:

First Named Applicant: Thomas Bednar

Attorney Docket Number: BUR920020107US1

Art Unit:

Examiner:

Search string: (6202191 or 6185722 or 6184477 or 6182272 or 6035111 or 6028440 or 6002857 or 5978572 or 5923089 or 5793643 or 5404310 or 5283753 or 5272645 or 5145800 or 5040144).pn

US Patent Documents

Note: Applicant is not required to submit a paper copy of cited US Patent Documents

init	Cite.No.	Patent No.	Date	Patentee	Kind	Class	Subclass
HR	1	6202191	2001-03-27	Filippi et al			
HR	2	6185722	2001-02-06	Darden et al			
HR	3	6184477	2001-02-06	Tanahashi			
HR	4	6182272	2001-01-30	Andreev et al			
HR	5	6035111	2000-03-07	Suzuki et al			
HR	6	6028440	2000-02-22	Roethig et al			
HR	7	6002857	1999-12-14	Ramachandran			
HR	8	5978572	1999-11-02	Toyonaga et al			
HR	9	5923089	1999-07-13	Yao et al			
HR	10	5793643	1998-08-11	Cai			
HR	11	5404310	1995-04-04	Mitsuhashi			
HR	12	5283753	1994-02-01	Schucker et al			
HR	13	5272645	1993-12-21	Kawakami et al			
HR	14	5145800	1992-09-08	Arai et al			
HR	15	5040144	1991-08-13	Pelley et al			

Signature

Examiner Name	Date
Helen Rossoshek	09/27/2005

FORM PTO-1449 (Modified)

LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S *SUPPLEMENTAL* INFORMATION DISCLOSURE STATEMENT

Page 1 of 1

(Use several sheets if necessary.)

ATTY DOCKET NO.	SERIAL NO.
BUR9200200107US1	10/604,995
APPLICANT: Bednar et al.	
FILING DATE: 8/29/2003	GROUP: Not yet assigned

REFERENCE DESIGNATION

U.S. PATENT DOCUMENTS

EXAMINERS INITIALS		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPRO.)
	AA						
	AB						
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						
	AL						
	AM						
	AN						
	AO						

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO
	AO							

OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)

HR	AP		INCREASED CHIP WIREABILITY THROUGH MORE EFFICIENT POWER DISTRIBUTION, IBM Technical Disclosure Bulletin, Vol. 38, No. 09, pgs. 243-245, September 1995.

EXAMINER Helen Rossoshek

DATE CONSIDERED 09/27/05

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.